WHAT IS CLAIMED IS:

1. For use with a power converter having a main active clamp circuit associated with a main power switch coupled to a primary winding of a transformer and a rectifier switch coupled to a secondary winding of said transformer, said main power switch configured to conduct during a main conduction period of said power converter and said rectifier switch configured to conduct during an auxiliary conduction period of said power converter, a gate driver, comprising:

a DC offset bias circuit, coupled to a secondary winding of said transformer, configured to provide a gate drive signal having a DC bias voltage to a gate terminal of said rectifier switch.

2. The gate driver as recited in Claim 1 further comprising a resistor, coupled in series with said gate terminal of said rectifier switch, configured to extend a transition time of said rectifier switch from a conducting state during said auxiliary conduction period to a non-conducting state.

3. The gate driver as recited in Claim 1 wherein said DC offset bias circuit comprises a battery.

4. The gate driver as recited in Claim 1 wherein said DC offset bias circuit comprises a zener diode.

5. The gate driver as recited in Claim 4 wherein said DC offset bias circuit further comprises a capacitor coupled in parallel to said zener diode.

6. The gate driver as recited in Claim 4 wherein said DC offset bias circuit further comprises a resistor coupled to said zener diode.

7. The gate driver as recited in Claim 1 wherein said rectifier switch is a synchronous rectifier switch.

8. For use with a power converter having a main active clamp circuit associated with a main power switch coupled to a primary winding of a transformer and a rectifier switch coupled to a secondary winding of said transformer, said main power switch conducts during a main conduction period of said power converter and said rectifier switch conducts during an auxiliary conduction period of said power converter, a method of driving said rectifier switch, comprising:

coupling a DC offset bias circuit to a secondary winding of said transformer and a gate terminal of said rectifier switch; and

providing a gate drive signal having a DC bias voltage via said DC offset bias circuit to a gate terminal of said rectifier switch.

9. The method as recited in Claim 8 further comprising extending a transition time of said rectifier switch from a conducting state during said auxiliary conduction period to a non-conducting state.

10. The method as recited in Claim 8 wherein said DC offset bias circuit comprises a battery to provide said DC bias voltage.

11. The method as recited in Claim 8 wherein said DC offset bias circuit comprises a zener diode.

12. The method as recited in Claim 11 wherein said DC offset bias circuit further comprises a capacitor coupled in parallel to said zener diode, said zener diode and capacitor cooperating to provide said DC bias voltage.

13. The method as recited in Claim 11 further comprising providing a bias current to said zener diode.

14. A power converter, comprising:

a main power switch coupled to an input of said power converter that conducts during a main conduction period of said power converter;

a main active clamp circuit associated with said main power switch;

a transformer having a primary winding coupled to said main power switch;

a rectifier coupled to a secondary winding of said transformer and including a rectifier switch that conducts during an auxiliary conduction period of said power converter; and

a gate driver, including:

a DC offset bias circuit, coupled to a secondary winding of said transformer, that provides a gate drive signal having a DC bias voltage to a gate terminal of said rectifier switch.

15. The power converter as recited in Claim 14 wherein said gate driver further comprises a resistor, coupled in series with said gate terminal of said rectifier switch, that extends a transition time of said rectifier switch from a conducting state during said auxiliary conduction period to a non-conducting state.

16. The power converter as recited in Claim 14 wherein said DC offset bias circuit comprises a battery.

17. The power converter as recited in Claim 14 wherein said DC offset bias circuit comprises a zener diode coupled in parallel to a capacitor, said DC offset bias circuit further comprising a resistor coupled to said zener diode.

18. The power converter as recited in Claim 14 wherein said rectifier switch is a synchronous rectifier switch.

19. The power converter as recited in Claim 14 further comprising an auxiliary active clamp circuit associated with said rectifier switch.

20. The power converter as recited in Claim 19 wherein said auxiliary active clamp circuit, comprises:

an auxiliary clamp capacitor, coupled across said rectifier switch, that stores a clamping voltage substantially equal to an off-state voltage of said rectifier switch; and

an auxiliary clamp switch, coupled in series with said auxiliary clamp capacitor, that receives a drive signal from a secondary winding of said transformer and conducts during said main conduction period thereby clamping a voltage across said rectifier switch at about said clamping voltage.